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Docket No. 49855-CPA (70904)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	H. Washio et al.		
U.S. SERIAL NO.:	09/578,440	GROUP:	2674
FILED:	May 25, 2000	EXAMINER:	A. Abdulselam
FOR:	SHIFT REGISTER AND IMAGE DISPLAY APPARATUS USING THE SAME		

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on this date July 21, 2004 in an envelope as "Express Mail Post Office to Addressee," mailing Label Number EV438970133US addressed to the: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

By: Michelle P. Chicos
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Sir:

RESPONSE TO OFFICE ACTION

Applicants appreciate the courtesy extended by Examiner Abdulselam and Examiner Wu in conducting a personal interview with Applicants' representative on July 6, 2004. During the interview, Applicants' representative explained that the cited combination of references does not teach or suggest a shift register including a plurality of level shifters, one of the level shifters corresponding to each block of flip flops, as recited in the Applicants' claimed invention. Examiner Abdulselam and Examiner Wu agreed to withdraw the rejection, in response to Applicants' written remarks.

Claim 1, e.g., recites a shift register having a plurality of flip flops divided into a plurality of blocks and a plurality of level shifters, one of the level shifters corresponding to each of the blocks, where each level shifter increases the voltage of the clock signal and applies the clock

signal to the corresponding block of flip flops. Similarly, claims 20, 26, and 27 recite a level shifter corresponding to a predetermined number or block of flip flops.

Claims 1-31 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,232,945 to Moriyama et al. (hereinafter "Moriyama") in view of U.S. Patent 6,683,605 to Bi et al. ("Bi") and U.S. Patent 5,210,712 to Saito.

Moriyama fails to teach or suggest a plurality of flip flops for level-shifting a clock signal, where each level shifter corresponds to a predetermined number or block of flip flops.

On page 3 of the Office Action, it was acknowledged that "Moriyama does not teach a plurality of level shifters such that each level shifter increases the voltage of the clock signal, and applies the clock signal to the corresponding block of flip flops."

Bi fails to remedy the deficiencies of Moriyama. In particular, Bi does not teach or suggest a plurality of level shifters, each level shifter corresponding to one or more flip flops.

In Bi, a video controller 113A requires two separate clock signals: 14 MHz and 32 kHz, which are supplied by a clock generator 398 via a signal level translator **542** (see col. 31, lines 25-31). It is noted that reference numeral 452 in column 31, lines 31 and 34 is a typographical error, where the correct reference numeral 542 is provided in FIG. 14A and elsewhere in the specification.

The signal level translator 542 is used to convert 3-volt clock output signals (e.g. 14 MHz and 32 kHz) to 5-volt levels (see column 24, lines 65-67). The signal level translator 542 depicted in FIG. 14A is a single component that receives multiple 3-volt address bits and converts them to 5-volt address bits (see column 25, lines 4-16).

Bi does not teach or suggest a plurality of level shifters, each level shifter corresponding to one or more flip flops. Even if the signal level translator 542 was considered a "level shifter"

and somehow combined with the logic circuit of Moriyama, because the signal level translator 542 receives multiple bits, only one signal level translator 542 would be provided for the plurality of "flip flops" in Moriyama.

In contrast, the Applicants' claimed invention requires a plurality of level shifters, each level shifter corresponding to one or more flip flops. In accordance with the Applicants' claimed invention, by providing each level shifter corresponding to a predetermined number or block of flip flops, it is possible to shorten a distance between the level shifter and the corresponding flip flop(s), thereby reducing power consumption (see page 20 of Applicants' specification).

Saito also fails to teach or suggest a plurality of level shifters, each level shifter corresponding to one or more flip flops. FIG. 4 and col. 8, lines 14-25, as cited in the Office Action, disclose only a single level shifter 1. Therefore, Saito could not be combined with Moriyama to somehow produce the Applicants' claimed invention.

For at least the reasons discussed above, the combination of Moriyama in view of Bi and Saito does not teach or suggest the Applicants' invention as recited in claims 1, 20, 26, and 27.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

EDWARDS & ANGELL, LLP

Date: July 21, 2004

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